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10EC/TE71

Seventh Semester B.E. Degree Examination, Dec.2017/Jan.2018

Computer Communication Networks

Time: 3 hrs. Max. Marks:100

Note: ***Answer any FIVE full questions, selecting at least TWO questions from each part.***

PART – A

1 a. Describe the ISO-OSI reference model of a computer network. Discuss the function of each layer. **(10 Marks)**

b. Match the following to one or more layers in OSI model:
(i) Route determination
(ii) Flow control
(iii) Interface to transmission media
(iv) Provides access for end user
(v) Format and code conversion services **(05 Marks)**

c. With necessary diagram, explain the DMT used in ADSL. **(05 Marks)**

2 a. Explain with suitable examples:
(i) Byte stuffing and unstuffing
(ii) Bit stuffing and unstuffing. **(10 Marks)**

b. In a stop and wait ARQ system, the bandwidth of line is 1 Mbps and it takes 20 ms to make a round trip. What is the bandwidth delay product? If the system data frames are of 1000 bit length, what is the utilization percentage of link? What is the channel utilization percentage of link if the protocol that can send upto 15 K frames before stopping and worrying about acknowledgement? **(05 Marks)**

c. Explain the I-Frame and V-Frame in HDLC protocol. **(05 Marks)**

3 a. Compare pure ALOHA with slotted ALOHA. What are the reasons for poor channel utilization in ALOHA systems? How the same is approved in CSMA? **(08 Marks)**

b. Mention the different types controlled access protocols used in multiple access protocols. Explain each briefly. **(08 Marks)**

c. Prove that a receiving station can get the data sent by a specific sender if it multiplies the entire data on the channel by the sender's chip code and then divided by its number of stations. (Assume N = 4). **(04 Marks)**

4 a. Explain the four different types of Ethernet format briefly. **(10 Marks)**

b. With neat diagram of Bluetooth layer. Explain the three types of frames in base band layers. **(10 Marks)**

PART – B

5 a. List the five different categories of connecting devices operating at different layers. Explain briefly. **(10 Marks)**

b. (i) What is the basis for membership in a VLAN?
(ii) How are the station configured into different VLAN's? **(10 Marks)**

6 a. Find the range of Address in the following blocks:
(i) 123.56.77.32/29
(ii) 200.17.21.128/27
(iii) 17.34.16.0/23
(iv) 180.34.64.64/30 **(10 Marks)**

b. Explain the IPV4 datagram format. **(10 Marks)**

7 a. Explain the Dijkstra algorithm for the given network [Fig.Q7(a)]:

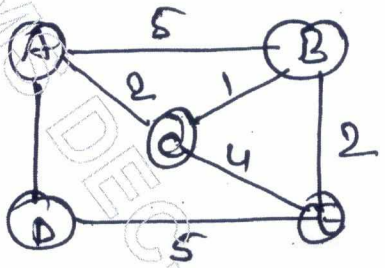

Fig.Q7(a) **(10 Marks)**

b. Explain the different techniques used to forward packet from source to destinations. **(10 Marks)**

8 a. How does recursion resolution differ from iterative resolution? **(05 Marks)**

b. Write short notes on:
(i) User Datagram Packet Format (UDP)
(ii) Features of TCP **(10 Marks)**

c. Suppose a TCP connection is transferring a file of 5000 bytes, the first byte is numbered 10,001. What are the sequence number of each segment, if data are sent in five segments each carrying 1000 bytes? **(05 Marks)**

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10EC/TE72

Seventh Semester B.E. Degree Examination, Dec.2017/Jan.2018
Optical Fiber Communication

Time: 3 hrs. Max. Marks:100

Note: ***Answer FIVE full questions, selecting at least TWO questions from each part.***

PART – A

1 a. Derive the expression for Numerical Aparture using ray theory. **(07 Marks)**

b. In brief discuss the different design approaches for single-mode fibers. **(07 Marks)**

c. A graded index fiber has a core with a parabolic-index profile which has a diameter of 50 μm. The fiber has a numerical aperture of 0.2. Estimate the total number of guided modes propagating in the fiber when it is operating at a wavelength of 1 μm. **(06 Marks)**

2 a. In brief explain linear scattering losses. **(07 Marks)**

b. Derive the expression for rms-pulse broadening due to intermodal dispersion in a step index fiber. **(08 Marks)**

c. A multimode graded index fiber exhibits total pulse broadening of 0.1 μ.s over a distance of 15 km. Estimate the following:
(i) Maximum possible bandwidth on the link assuming no ISI.
(ii) Pulse dispersion per km.
(iii) BW-length product for the fiber. **(05 Marks)**

3 a. Explain the GaAlAs double-heterojunction LED structure. **(07 Marks)**

b. Explain the structure of RAPD and its working. **(08 Marks)**

c. A double-heterojunction structure in GaAsP LED emitting a peak wavelength of 1310 nm has a radiative and non radiative recombination times of 30 ns and 100 ns respectively. The drive current is 40 mA. Estimate the
(i) Bulk recombination life time.
(ii) Internal power level. **(05 Marks)**

4 a. Explain lensing schemes for coupling improvement. **(07 Marks)**

b. List out the requirements that a good connector design has to meet. **(07 Marks)**

c. A GaAs optical source with refractive index of 3.6 is coupled to a silica fiber that has a refractive index of 1.48. If the fiber ends face and source are in close physical contact. Estimate Fresnel reflection at the interface and power loss in dB. **(06 Marks)**

PART – B

5 a. In brief explain basic structure of an optical receiver. **(08 Marks)**

b. Discuss the features of Eye-pattern. **(07 Marks)**

c. Write short note on "Burst-mode receiver". **(05 Marks)**

6 a. Derive the expression for rise-time budget analysis. **(08 Marks)**

b. In brief explain multi channel AM technique. **(07 Marks)**

c. Write a short note on "Microwave photonics". **(05 Marks)**

7 a. Explain in brief design and operation of polarization – independent isolator. **(08 Marks)**

b. Explain in brief operational principle and implementation of WDM with diagram. **(07 Marks)**

c. Write a short note on "MEMS technology". **(05 Marks)**

8 a. Explain three possible configurations of a EDFA. **(08 Marks)**

b. Explain the SONET/SDH frame format. **(07 Marks)**

c. Write a short note on "Semiconductor Optical Amplifiers" **(05 Marks)**

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10EC73

Seventh Semester B.E. Degree Examination, Dec.2017/Jan.2018
Power Electronics

Time: 3 hrs. Max. Marks:100

Note: ***Answer FIVE full questions, selecting at least TWO questions from each part.***

PART – A

1 a. Mention at least one power semiconductor device for,
(i) Uncontrolled turn on and off.
(ii) Controlled turn on and uncontrolled turn off.
(iii) Controlled turn on and turn off.
(iv) Bi-directional control turn on and uncontrolled turn off. **(02 Marks)**

b. Write symbol and characteristics features of, (i) SCR (ii) MCT (iii) SITH (iv) MOSFET **(08 Marks)**

c. Explain different types of power electronics circuits with their input and output waveforms. **(10 Marks)**

2 a. Explain any three base drive control circuits of power BJT. **(10 Marks)**

b. Explain switching characteristics of IGBT. **(04 Marks)**

c. Discuss switching limits of power transistors. **(06 Marks)**

3 a. Explain different ways of thyristor turn-on methods and discuss turn on dynamic characteristics. **(10 Marks)**

b. Calculate the required parameters for snubber circuit to provide $\frac{dv}{dt}$ protection to a SCR used in a converter. The SCR has a maximum $\frac{dv}{dt}$ capability of 60 V/μsec. The input has a peak value of 425 volts and the source inductance is 0.2 mH. Given damping factor $\sigma = 0.65$. **(04 Marks)**

c. With neat circuit diagram and waveforms, explain RC-Halfwave firing circuit. **(06 Marks)**

4 a. Explain the operation of single-phase full converter with neat circuit diagram and waveforms for a ripple free and continuous load current. Derive the expression for average and rms output voltage. **(10 Marks)**

b. Explain how a dual converter works in all four quadrants. **(06 Marks)**

c. The single phase dual converter is operated from a 120 V, 60 Hz supply and delivers ripple free average current of $I_{dc} = 20$ A. The circulating inductance is $L_r = 5$mH and delay angles are $\alpha_1 = 30^\circ$ and $\alpha_2 = 150^\circ$. Calculate the peak circulating current and peak current of converter 1. **(04 Marks)**

PART – B

5 a. Explain the operation of an auxillary voltage commutation circuit using single auxillary thyristor. Derive an expression for commutating components. **(10 Marks)**

b. In the circuit shown in Fig. Q5 (b), the main SCR T_1 is to be turned off for atleast 140 μsec. For proper commutation determine the values of R and C. Given holding current of an auxillary SCR T_2 is 3.5 mA. **(04 Marks)**

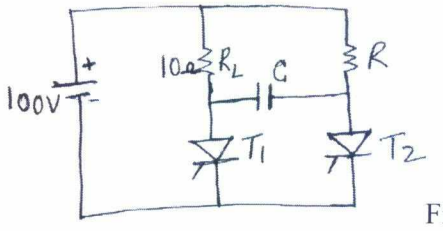

Fig. Q5 (b)

c. For the commutation circuit shown in Fig. Q5 (c). Check whether SCR is commutated successfully. If not what could be the minimum value of capacitor to be connected for successful commutation. Typical turn off time of SCR is 50 μsec. **(06 Marks)**

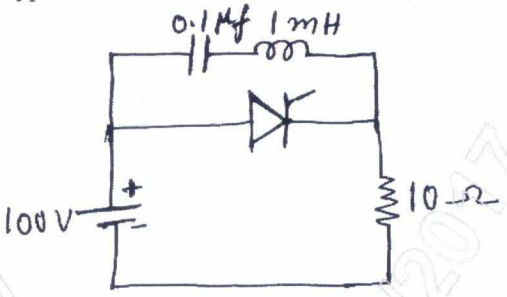

Fig. Q5 (c)

6 a. Explain the operation of single phase unidirectional AC-voltage controller with resistive load. Derive the expression for rms output voltage. **(10 Marks)**

b. Explain why a single short duration gating pulse is not suitable for inductive load. Also give the remedy for the same. **(06 Marks)**

c. The AC-voltage controller uses ON-OFF control for heating a resistive load of R = 4 Ω and input voltage is V_S = 230V , 50 Hz. If the desired output power P_0 = 3 kW. Determine (i) the duty cycle K and (ii) Input PF. **(04 Marks)**

7 a. Explain the performance parameters of choppers. **(04 Marks)**

b. Input to the step-up chopper is 200 V. The output required is 600 V. If the conducting time of thyristor is 200 μsec. Compute (i) Chopping frequency (ii) If pulse width is halved for constant frequency find the new output voltage. **(06 Marks)**

c. With the help of circuit diagram and waveforms, explain the working of a Buck regulator. Derive the expression for peak-to-peak ripple current of the inductors. **(10 Marks)**

8 a. Explain the operation of single-phase half bridge inverter with feedback diodes. Derive the expression for rms output voltage. **(10 Marks)**

b. With neat circuit diagram, explain thyristorized current source inverter. **(06 Marks)**

c. Compare between voltage source inverter and current source inverter. **(04 Marks)**

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10EC74

Seventh Semester B.E. Degree Examination, Dec.2017/Jan.2018
Embedded System Design

Time: 3 hrs. Max. Marks:100

Note: ***Answer any FIVE full questions, selecting at least TWO questions from each part.***

PART – A

1 a. Define an embedded system. Explain the traditional approach of an embedded system design with neat flow diagram. **(08 Marks)**

b. What are the different computing engines available in the embedded system? Explain briefly. **(06 Marks)**

c. A microprocessor support 144 instruction and has 256 register. Write the instruction format using 32-bit instruction register for 1-adder, 2-adder and 3-adder using big Endian and little Endian. **(06 Marks)**

2 a. Explain the various types of addressing modes used in embedded system design with example. **(06 Marks)**

b. What are the basic operation can be performed on a register and also explain RTN model for microprocessor data path and memory interface. **(08 Marks)**

c. What is state diagram? Briefly explain FSM (Finite State Machine) with a block diagram. **(06 Marks)**

3 a. Discuss the classification of memory. **(06 Marks)**

b. Explain the various schemes available in DMA. **(06 Marks)**

c. What do you mean 'cache hit' and 'cache miss' and also illustrate cache direct mapping methods. **(08 Marks)**

4 a. Explain waterfall life cycle model along with steps. **(08 Marks)**

b. Briefly explain the various kinds of cohesion. **(06 Marks)**

c. Discuss functional versus architecture model. **(06 Marks)**

PART – B

5 a. What is operating system? Explain the roles and responsibilities of each component. **(08 Marks)**

b. Explain about (i) process and threads, (ii) sharing resources. **(06 Marks)**

c. What are the various kinds of stack used in embedded application? Briefly explain. **(06 Marks)**

6 a. What is TCB? Also illustrate TCB and its C-code structure. **(08 Marks)**

b. Explain about FOREGROUND and BACKGROUND systems. **(05 Marks)**

c. Describe memory management revisited. **(07 Marks)**

7 a. What do you mean by 'performance' or 'efficiency measure' in an embedded system? **(06 Marks)**

b. Analyze and explain the following program using looping constructs flow:

```
Program code: int sum = 0;
              for (int i = 0; i < N; i++)
                  sum = sum + i;
```

(08 Marks)

c. Briefly explain the basic fundamental operations in DATA STRUCTURE. **(06 Marks)**

8 a. What are hardware accelerators? Explain the use of hardware accelerator with example. **(06 Marks)**

b. Explain the basic elements used in analyzing flow of control. **(08 Marks)**

c. How do you reduce power consumption in software? **(06 Marks)**

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10EC751

Seventh Semester B.E. Degree Examination, Dec.2017/Jan.2018
DSP Algorithms and Architecture

Time: 3 hrs. Max. Marks:100

Note: ***Answer any FIVE full questions, selecting atleast TWO questions from each part.***

PART – A

1 a. With the help of block diagram and equations explain decimation and interpolation process. Also determine the interpolated sequence y(m), if the signal sequence x(n) = {0, 2, 4, 6, 8} is interpolated using the interpolation filter sequence b_k = {0.5, 1, 0.5}. Interpolation factor L = 2. **(10 Marks)**

b. Explain with the block diagram of a DSP system. Also draw the typical signals in a DSP scheme. **(08 Marks)**

c. Assuming x(k) as a complex sequence, determine the number of complex and real mulitplies for computing DFT, using direct and radix – 2 FFT algorithms. assume N = 1024. **(02 Marks)**

2 a. Mention the basic features that should be provided in the DSP architecture to be used to implement the following N^{th} order FIR filter $y(n) = \sum_{i=0}^{N-1} h(i)x(n-i)$; n = 0, 1, 2, - - - . **(04 Marks)**

b. Explain the register pointer updating algorithm for circular buffer. **(06 Marks)**

c. With relevant block diagram, explain the various features of arithmetic and logic unit of DSP processor. **(06 Marks)**

d. Write a note on organization of the on-chip memory. **(04 Marks)**

3 a. Compare the architectural features of TMS320C25 and DSP56000. **(08 Marks)**

b. Draw the functional diagram of the barrel shifter of TMS320C54XX processor and explain the significance of each block. **(08 Marks)**

c. Assuming the current contents of AR3 to be 200h, what will be its contents after each of the following TMS320C54XX addressing modes is used. Assume that the contents of ARO are 40h i) *AR3 – 0 ii) *AR3 + iii) *+AR3(50h) iv) *AR3 – OB. **(04 Marks)**

4 a. Explain the pipeline operation of TMS320C54XX processor. Show the pipeline operation of the following sequence of instructions if the initial value of AR3 is 85h and the values stored in memory location 85h, 86h, 87h are 5, 6 and 7.

```
LD  * AR3 +, A
ADD  # 1000h, A
STL A, * AR3 +.
```

(08 Marks)

b. Write the TCR register format and explain the functions of the various bits in the TCR register. **(06 Marks)**

c. Write a program to compute the sum of three product terms given by the equation : $y(n) = h_0x(n) + h_1x(n-1) + h_2x(n-2)$ where x(n), x(n – 1), x(n – 2) are data samples stored at three successive data memory locations h_0, h_1, h_2 are constants stored in data memory. Use direct addressing mode. **(06 Marks)**

PART – B

5 a. Represent each of the following as 16 – bit numbers in the desired Q – notation :
   i) 0.3125 as a Q_{15} number
   ii) –0.3125 as a Q_{15} number
   iii) 3.125 as a Q_7 number
   iv) –352 as a Q_0 number. **(04 Marks)**

b. Write a TMS320C54XX program for the implementation of an interpolating FIR filter of length 15 and interpolating factor 5. **(08 Marks)**

c. Write a program to multiply two Q_{15} numbers in TMS320C54XX processor. **(04 Marks)**

d. Briefly explain IIR filters. With the help of block diagram, explain second order IIR filters. **(04 Marks)**

6 a. Determine the following for a 128 – point FFT computations :
   i) Number of stages
   ii) Number of butterflies in each stage
   iii) Number of butterflies needed for the entire computation
   iv) Number of butterflies that need no twiddle factor. **(04 Marks)**

b. Write subroutine for bit reverse address generation and explain the same. **(06 Marks)**

c. Explain the butterfly computation in DIT FFT algorithm and write a subroutine that implements the butterfly computation. **(10 Marks)**

7 a. Draw the timing diagram of the memory interface signals for a read – read –write sequence of operations. Also explain the purpose of each signal. **(06 Marks)**

b. Explain the register sub-addressing technique for configuring DMA. **(04 Marks)**

c. Interface the TMS320C54XX to a 10 –bit ADC(TLC1550) and an 8 bit DAC (TLC7524). The sampled signal read from the ADC is to be written to the DAC after adjusting its size. The start of conversion is initiated by the TOUT signal. Write a flowchart for main program and interrupt service routine and also write the program. **(10 Marks)**

8 a. With a neat block diagram and timing diagram for transmit and receive operation, explain the signals involved in synchronous serial interface. **(08 Marks)**

b. With the help of block diagram, explain DSP based biotelemetry receiver system. **(06 Marks)**

c. Explain the image compression and reconstruction using JPEG encoder and decoder. **(06 Marks)**

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10EC/TE762

Seventh Semester B.E. Degree Examination, Dec.2017/Jan.2018
Real Time Systems

Time: 3 hrs. Max. Marks:100

Note: ***Answer any FIVE full questions, selecting atleast TWO questions from each part.***

PART – A

1 a. What is real time system? Explain general computer control system with neat block diagram **(08 Marks)**

b. Define the term "Time constraint"? How are RTS classified based on time constraint? **(06 Marks)**

c. Discuss different types of programs in system design. **(06 Marks)**

2 a. With an example explain sequence control n field application and write the block diagram of typical chemical batch processing. **(10 Marks)**

b. Explain dual computer scheme. **(05 Marks)**

c. Explain DDC and its advantages with neat diagram. **(05 Marks)**

3 a. Explain interrupt vectoring using priority encoder circuit. **(06 Marks)**

b. Explain digital interfaces. **(08 Marks)**

c. Explain different LAN topologies. **(06 Marks)**

4 a. List and explain various requirements in programming languages used in real time applications. **(12 Marks)**

b. Explain simple table driven approach used for application oriented software. **(08 Marks)**

PART – B

5 a. What are the functions of task states with task state diagram? **(10 Marks)**

b. Explain different scheduling strategies. **(06 Marks)**

c. Explain : i) Task chaining ii) Task swapping. **(04 Marks)**

6 a. Explain the problem of shared memory. How semaphores are used to overcome this problem. **(10 Marks)**

b. Explain live-lock, deadlock and indefinite postponement in brief. **(06 Marks)**

c. Explain : i) pool ii) channel. **(04 Marks)**

7 a. With neat flow chart, describe single program approach with reference to RTS design. **(10 Marks)**

b. Explain software design of RTS using software module. **(10 Marks)**

8 a. Explain functional specifications with respect to a drying oven. **(08 Marks)**

b. Explain Yourdon methodology. **(06 Marks)**

c. Differentiate between the ward and Mellor method and Hatley and Pirabhai methodologies. **(06 Marks)**

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